Sofia Test Procedure

SOFIA circuit description

Sofia has inside four PC board named as the title of the relative schematic which are:

- 1) SOFIA MICROCONTROLLER AND CODEC (3 sheets)
- 2) SOFIA HT (1 sheet)
- 3) SOFIA POWER SUPPLY (1 sheet)
- 4) SOFIA SOKET (It has no schematic)

SOFIA POWER SUPPLY

SOFIA HT

Receives power supply with four separate two pole connectors, J1 J2 J3 and J5, is connected with SOFAI SOKET with an 8 pole connector J6, is connected with SOFIA MICROCONTROLLER AND CODEC with a 20 pole flat connection. Contains 6 functional blocks:

- 1) Anode high voltage driver
- 2) Screen grid high voltage driver
- 3) Power fets driver
- 4) Heather high current driver
- 5) Grid driver
- 6) Power supply conditioner

SOFIA HT Anode hi voltage driver receives power from J1 which drives directly a step down voltage controlled switching regulator based on U1, the step down regulator and U5 that furnish feedback to U1 comparing the output hi voltage VAN and the control voltage VCAN that comes from SOFIA MICROCONTROLLER CODEC. U1's output, DC converted by L1 and C12, ranges from 0 to about 35V and drives the centre tap of TR1 step up transformer primary. Q1 and Q2 are drain connected with T1 and acts as push pull driver and are grid controlled by the Power fets driver described below. TR1 secondary voltage is applied to a voltage doubler and rectifier based on D2 D3 C6 and C7. One side of this stage is ground connected trough R9 that acts as current sensing resistor; the other side is sent to the tube anode through J6 and to U5 via R5 and R6 voltage divider; it ranges from 0 to 700V.

SOFIA HT Screen grid hi voltage driver is an exact replica of the previous stage. J2, U10, Q3, Q4, T2 and U6 are the main components involved. VCGR2 is the control voltage, VGR2 the output.

SOFIA HT Power fets driver relies on U2, U3, U4, R13, R14, C16 and C23. U2, a flip flop, is used as frequency divider and opposite polarity square waves generator; clock is fed from U11 drive signal, a 100kHz pulse signal. Q+ and Q- drive U3 that with R13, R14, C16 and C23 make the low state of the square waves a little shorter then the high state. This signal inverted by U4 drives the fets grid avoiding overlap of conduction in the push pull stage due to fets Toff time.

SOFIA HT Heather high current driver relies on U7 and U8 and is very similar to the step down voltage controlled switching regulator described above. This block is separately supplied by J3 and receives its control voltage VCFIL from SOFIA MICROCONTROLLER CODEC via J4. Its output VFIL goes to the tube heather via J6 and SOFIA SOKET and ranges from 0 to 24V; heather return is ground connected with R44 used as current sensing resistor.

SOFIA HT Grid driver relies on U9, Q5 and associated passive components. Receives the control voltage VCGR1 and supplies the tube grid voltage VGR1. Q5 collector is connected to a high negative voltage (see below) trough R30. Its output ranges from +10V to -150V.

SOFIA HT Power supply conditioner receives the not regulated DC power supply via J5 connector. U11 together with TR3 acts as a switching flyback converter providing the +15 and -15V. +5V are obtained from +15V trough U12, a 7805 linear regulator. The switching signal at U11 pin 4 drives both the TR3 transformer and a series of four diodescapacitors voltage doubler (C52..C56 and D19.. D26) that provides the -170V for the grid driver.

SOFIA test description

To perform the following tests, you have to connect the test load to Sofia's socket, and use the SofCalib.exe software.

Sofia Test Load:

This load is built with 3 resistors connected as follows:

5KOhm 100W resistor between plate and ground.

5KOhm 100W resistor between screen and cathode.

24 Ohm 50W resistor between heater+ and heater-.

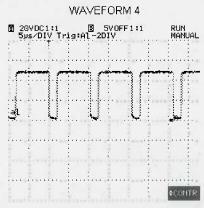
Supply Voltage Test:

First of all check supply voltage (on fuse FU3) for 38.5 V (± 10%) no charge.

Then check the other supply voltage:

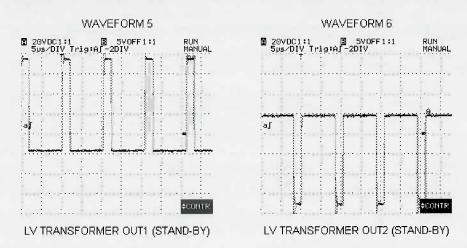
- i) $V1 = 16.3 \text{ V } (\pm 10\%) \text{ on pin 7 of U6}.$
- ii) $V2 = -17.3 \text{ V } (\pm 10\%) \text{ on pin 4 of U6.}$
- iii) $V3 = 5 V (\pm 3\%)$ on pin 14 of U4.
- iv) $V4 = -170 \text{ V} (\pm 10\%) \text{ on TP5 (pin 2 of R30)}.$

The waveform on TP1 (pin 1 of R42) must be as in Figure WAVEFORM 4.



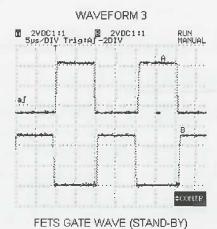
LV TRANSFORMER DRIVE (STAND-BY)

Waveform on D17 Cathode, Figure WAVEFORM 5; on D18 Anode, Figure WAVEFORM 6.



Fets Drive Test:

The Gate signal on fets Q1 (Trace A) + Q2 (Trace B) and Q3 (Trace A) + Q4 (Trace B) is shown in figure WAVEFORM 3.



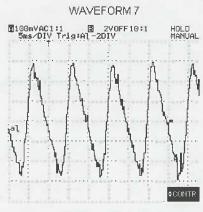
Working Voltage Test:

These test have to be executed under control of SofClib.exe (see instruction for help) software.

Power supply ripple (menu option 'A'):

The control software (SofCali.exe) sets Plate Voltage at 200 V, Screen Voltage at 200 V and Heater Voltage at 24 V.

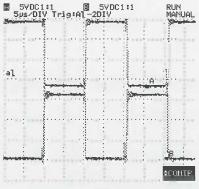
Measure supply voltage at 36 V (\pm 10%) on fuse FU3. Make sure the wave is good as shown in Figure WAVEFORM 7.



POWER SUPPLY RIPPLE (TEST 1)

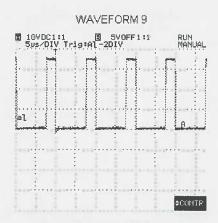
The wave on drain pin of Q1 (trace A) & Q2 (trace B) Fets is shown in Figure WAVEFORM 8.





FETS DRAIN WAVE (TEST 1)

Wave on TP3 (D1 Case) is in Figure WAVEFORM 9.



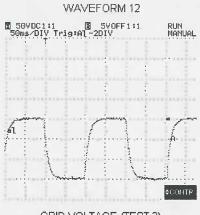
HT SHOTKY OUT WAVE (TEST 1)

Static Grid Test (menu option 'B'):

The control software switch on grid voltage at -150 V. Measure V5=-182 V (± 10%) on TP6 (pin 1 of R41).

Grid Test (menu option 'C'):

The control software move the grid voltage, continuously, from 0 to -150 V, the output waveform is shown in Figure WAVEFORM 12.



GRID VOLTAGE (TEST 3)

Heater Test (menu option 'D'):

The control software move the heater voltage, continuously, from 0 to 24 V, the output waveform is shown in Figure WAVEFORM 13.

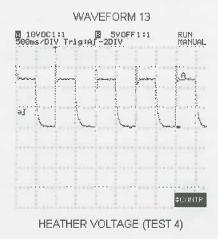
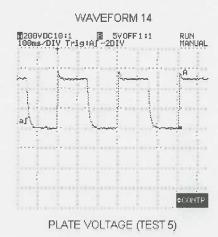


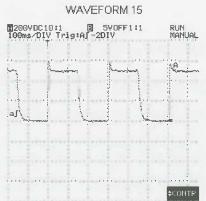
Plate Test (menu option 'E'):

The control software move the plate voltage, continuously, from 0 to 500 V, the output waveform is shown in Figure WAVEFORM 14_{\circ}



Screen Test (menu option 'F'):

The control software move the screen voltage, continuously, from 0 to 500 V, the output waveform is shown in Figure WAVEFORM 1



SCREEN GRID VOLTAGE (TEST 6)